Marked-up Version of Amended Paragraphs and Claims

Paragraph at page 14, lines 20-27:

Fig. 12 is a block diagram of a tester 21 embodiment that includes the decompressor 36, rather than providing it in the circuit 34. The tester decompresses the test pattern internally and transmits the decompressed test pattern to the CUT 24. Such [as]a tester [had]has advantages where testing time is not as critical and it is preferred not to add a decompressor to each circuit-under-test. Storage requirements are still reduced because compressed test patterns (rather than full test patterns) need only be stored. In addition, in a variation of the above tester embodiment, the compactors 38 can also be included in the tester 21 rather than the circuit 34. The circuit then returns uncompressed test responses to the tester. This further simplifies the circuit's design.

Replace the paragraph at page 12, lines 18-21 with the following:

The variable *x* denotes a "don't care" condition. Then a corresponding compressed test pattern can be determined by solving the following system of ten equations from Fig. 7 using any of a number of well-known techniques such as Gauss-Jordan elimination techniques. The selected equations correspond to the deterministically specified bits:

In the claims:

13. (Amended) The method of claim 1 wherein decompressing the compressed test pattern comprises generating [each bit]one or more bits of the decompressed pattern by logically combining two or more bits of the compressed test pattern.